REMARKS

By this amendment, claim 36 has been amended. Claims 1-35 have been previously cancelled. Accordingly, claims 36-45 are currently pending in the application, of which claim 36 is independent. Applicants respectfully submit that the above amendments do not add new matter to the application and are fully supported by the specification.

Entry of this Amendment is respectfully requested because it places the present application in condition for allowance, or in the alternative, better form for appeal. In view of the above Amendments and the following Remarks, Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Rejections Under 35 U.S.C. §103

Claims 36-45 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 5,259,881 issued to Edwards, *et al.* ("Edwards") in view of U. S. Patent No. 5,198,694 issued to Kwasnick, *et al.* ("Kwasnick"), further in view of U.S. Patent No. 5,578,520 issued to Zhang, *et al.* ("Zhang") and further in view of U.S. Patent No. 5,344,522 issued to Yagi, *et al.* ("Yagi"). Applicants respectfully traverse this rejection for at least the following reasons.

In this response, independent claim 36 has been amended to further recite "the apparatus *sequentially forms* the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer without breaking a vacuum and *without patterning the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer*".

An example of the newly added limitation is shown in Fig. 5 of the present application, in which the gate insulating layer 300, the amorphous silicon layer 400, the doped amorphous silicon 500 and the Cr layer 600 are sequentially formed *without being patterned* until the Cr layer 600 is formed on the doped amorphous silicon 500.

In this regard, Kwasnick discloses, in Fig. 5, the layer 30 of intrinsic amorphous silicon and the layer 32 of n+ amorphous silicon are patterned prior to forming the source/drain metallization 38. Thus, Kwasnick fails to disclose or suggest "the apparatus sequentially forms the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer without breaking a vacuum and *without patterning the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer*", as recited in claim 36.

Edward, Zhang and Yogi do not cure the deficiency from Kwasnick. Edwards is directed to a wafer processing cluster tool but is absolutely silent as to the specific sequence of forming the layers and whether sequentially formed layers are patterned or not. In fact, in Fig. 1, the wafer processing cluster tool includes the soft etch module 22, which suggests performing an etching step. Regarding the missing feature, the Examiner relied on Kwasnick. However, as explained above, Kwasnick also fails to disclose forming the layers without patterning them.

Zhang discloses a plurality of chambers arranged in series but does not disclose or suggest the specific sequence in forming the layers. In fact, the arrangement sequence of the chambers shown in Fig. 2 is such that the claimed specific sequence of forming the layers cannot be achieved.

Yogi discloses performing etching without breaking a vacuum but does not disclose the specific sequence of forming the layers and is silent whether sequentially formed layers are

patterned or not. In fact, the apparatus shown in Fig. 6 includes the latent image chamber 606 and the etch chamber 605, which suggest performing an etching step without breaking vacuum.

Thus, none of the cited references discloses or suggests "the apparatus *sequentially forms* the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer without breaking a vacuum and *without patterning the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer*", as claimed.

For this reason, it is submitted that claim 36 is patentable over them. Claims 37-45 that are dependent from claim 36 would be also patentable at least for the same reason. Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. §103(a) rejection of claims 36-45.

Claims 36-45 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 5,512,320 issued to Turner, *et al.* ("Turner") in view of Kwasnick further in view of Zhang and further in view of Yagi.

Amended independent claim 36 recites "the apparatus sequentially forms the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer without breaking a vacuum and *without patterning the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer*".

As previously mentioned, Kwasnick, Zhang and Yagi fail to disclose or suggest this claimed feature. Tuner discloses a vacuum processing apparatus comprising several CVD chambers and a heating chamber. However, Turner does not disclose or suggest the claimed specific sequence for forming the layers. Regarding this missing feature, the Examiner relied on Kwasnick but, as mentioned above, Kwasnick does not disclose "the apparatus sequentially

forms ... *without patterning the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer*".

Since none of the cited references discloses or suggests this claimed feature, it is submitted that claim 36 is patentable over them. Claims 37-45 that are dependent from claim 36 would be also patentable at least for the same reason. Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. §103(a) rejection of claims 36-45.

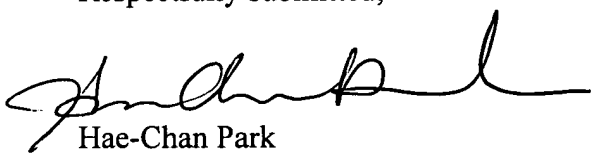
CONCLUSION

Applicants believe that a full and complete response has been made to the pending Office Action and respectfully submit that all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, Applicants respectfully submit that all pending claims are allowable and that the application is in condition for allowance.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact the Applicants' undersigned representative at the number below to expedite prosecution.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,



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